Amendments to the Specification:

Please replace paragraph [0053] in accordance with the following marked-up version of paragraph [0053]:

[0053] A third interlayer insulating layer 64 covering the pad conductive layer 60 and the MTJ layer 62 is formed in the second interlayer insulating layer 54. A via hole 66 exposing the MTJ layer 62 is formed on the third interlayer insulating layer 64. In addition, the bit line 70, which fills the via hole 66 and contacts the MTJ layer 62,~~6,~~ is formed on the third interlayer insulating layer 64. The bit line 70 may be perpendicular to the data line 52 and the gate stacking material 44.